Area and energy efficient 802.11ad LDPC decoding processor

Meng Li✉, Youngjoo Lee, Yanxiang Huang and Liesbet Van der Perre

The design of multi-Gbit/s low-density parity-check code (LDPC) decoders has become a hot topic in recent years to meet the growing demand of the transformation towards 4G. An area and energy efficient multi-Gbit/s LDPC decoder engine with a fully paralleled layered architecture based on an application-specific instruction set processor (ASIP) using Synopsys IP designer is presented. When the ASIP core is instantiated for 802.11ad, it achieved a throughput of up to 7 Gbit/s at three iterations with a latency of 95 ns, a record energy efficiency of 2.5 pJ/bit/iteration and an area efficiency of 54.5 Gbit/s/sq-m in CMOS 28 nm technology for the 1/2 rate, showing it to be competitive against published ASIC solutions.

Introduction: The low-density parity-check code (LDPC) is becoming popular and widely adopted in many new wireless standards because of its high error correction capability and matured solution of implementation. With the demands of the transformation towards the 4G telecommunication network, multiple standards are seeking to push their throughput towards higher Gbit/s. Meanwhile, the gigabit-wireless local area networks and IEEE 802.15.3c for the wireless personal area networks are almost ready for the market. Hence, the design of the multi-Gbit/s LDPC decoder has become a hot topic in recent years. However, designing a LDPC decoder with multi-gigabit throughput while maintaining low power consumption and low area, which is suitable for portable devices, is a big challenge.

The fully paralleled architecture, in which the number of check node function units (CFUs) and variable node function units (VFUs) reach the number of the parity check nodes and bit nodes, respectively, is one candidate for ultra-high throughput design; however, the routing congestion problem is becoming more severe as the technology nodes scale down. Although, the split-row method in [1] reduces the number of connection wires between CFUs and VFUs and hence saves area, it is still a challenge to design a fully paralleled decoder supporting all the coding rates.

Different from the fully paralleled architecture, the partial paralleled architecture, in which the CFUs and VFUs do not have one-to-one mapping to all the nodes in the Tanner graph, is another good candidate for multi-Gbit/s LDPC decoders. On the basis of the property of the LDPC codes, the designer can fully expand the parallelism of the VFUs or CFUs, which is called row-based mapping or column-based mapping in [2]. The partial paralleled architecture does not have the constraint from the decoding schedule, and both the flooding and layered schedules are applicable. The layered decoding schedule provides a faster convergence speed than the flooding schedule, due to intermediate utilisation of the posterior information. However, this property posts an implementation constraint on layer decoding. A pipelined decoding between layers is prohibitive for the row-based mapping architecture. In contrast to layered decoding, the flooding schedule needs pipelined layer or row decoding to compensate the low convergence speed to target ultra-high throughput.

In this Letter, we present a LDPC application-specific instruction set processor (ASIP) using the row-based architecture with layered scheduling, which is both area and energy efficient even compared with the ASIC design. The processor can easily be tuned to half-row- or quarter-row-based mapping for other quasi-cyclic (QC)-LDPC codes, which offers flexibility in the choice of different targeting throughputs and trade-offs between energy and area efficiency, and will speed up the time to market.

Architecture: The LDPC codes of 802.11ad are QC of each $Z = 42$ submatrix and support four coding rates, i.e. 1/2, 5/8, 3/4 and 13/16, with a coding length of 672. The proposed architecture is shown in Fig. 1, in which there are 762 VFUs and 42 CFUs. Sixteen slices are instantiated. Each slice consists of data memories, a barrel shifter and arithmetic computation elements, with a parallelism of 42. The maximum check node degree is 16, so each CFU needs to process maximum 16 *a priori* information which is sent from 16 different VFUs. Every layer decoding takes three cycles. In the first cycle, the *a posteriori* information is read from 16 data memories, then passed through the barrel shifter and finally subscribed by the 'extrinsic' information to produce the *a priori* information. In the second cycle, the CFU takes charge of finding the minimum absolute value and overall sign of all the fed in *a priori* information. In the last cycle, the output module generates the updated 'extrinsic' information, added by the pre-stored *a priori* information and then directly written back [3] to the data memories.

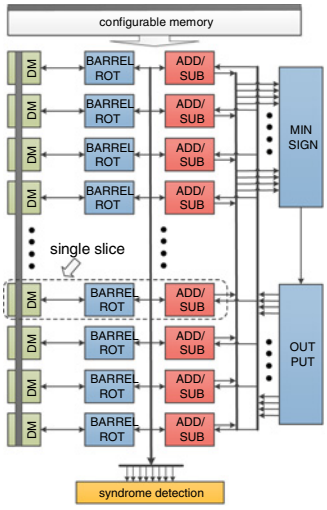

Fig. 1 *Top level fully layered LDPC decoder architecture*

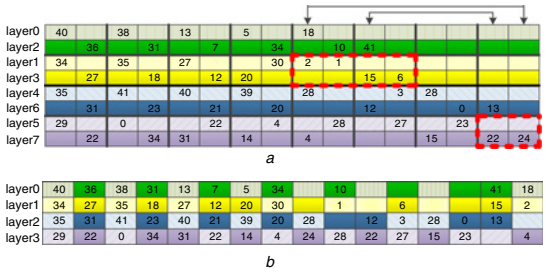

Fig. 2 *Parity check matrix of 802.11ad coding rate1/2 with re-ordering*

a Parity check matrix with row re-ordering
b Parity check matrix with row and column re-ordering with friendly routing and re-routing

The architecture is described as the SIMD/VLIW processor and there are four different instruction slots:

(1) scalar: initialisation and control,
(2) load–rotate–subtract: load *a posteriori* information, rotation and subtraction,
(3) min search: overall sign calculation and minimum, second minimum search,
(4) output–add–store: updated 'extrinsic' information generation, addition, store the updated *posteriori* information and syndrome calculation.

Since there is no pipeline between the two-layer decoding, the number of cycles per iteration is linear with the number of layers: 3N_layers + 1. (The last one cycle is required to rotate the *a posteriori* information vector back to serial order.) The increment of the number of layers for low coding rates reduces throughput significantly. Fortunately, the property of the parity check matrices of the coding rate 1/2 and 5/8 enables decoding two specific layers by row re-ordering in three cycles to boost the throughput. This is because the check nodes are not overlapped and the degree of each combined layer is no larger than 8. Therefore, each layer utilises half of the min-sum search tree hardware resources [4]. However, to route the two groups of *a priori* information in each layer to each half of the min-sum search tree and to re-route the two minimum values to the different slices is not straightforward, especially for the ones that are highlighted in the dotted boxes in Fig. 2. By applying certain column re-ordering at the parity part, in each combined layer, every two-bit node vector has a one-to-one mapping to the first half and second half of the min-sum search tree, which is shown in Fig. 2*b*. The regular routing and re-routing are preferable for the ASIP design and can

be realised by adding mux and de-mux after and before the information go through and to the ADD/SUB unit.

Implementation results: The design is synthesised and place-and-routed by 28 nm CMOS technology. Working at 400 MHz, the equivalent gate account is 282 K. Four coding rates are supported, and the ASIP processor achieves 9.26 Gbit/s data rate at three iterations for the coding rate 13/16 with the above configuration.

Comparison of the design and implementation results with the state-of-the-art LDPC decoders for the 802.11ad standard is shown in Table 1. In [5] the partial paralleled and partial-layer-pipelined architecture is adopted, which increases the throughput by carefully re-ordering the parity check matrix. To our best knowledge, [6, 7] are the only published taped-out designs for 802.11ad till now. It uses the row-based and frame-pipelined architecture with the flooding schedule and offers a wide range of throughput by using dynamic voltage and frequency scaling (DVFS). Since 6 Gbit/s is the maximum data rate for 802.11ad for the 1/2 coding rate, only the 6 Gbit/s mode is considered here. Different from the other works, [8] and this work are the ones done using ASIPs. The proposed processor can be easily instantiated for other QC-LDPC codes, e.g. 802.11ac. Moreover, by selecting the number of slices, the processor can be tuned to half-row- or quarter-row-based mapping, which offers the flexibility of choosing different throughput targets and trade-offs between energy and area efficiency.

Table 1: Implementation results comparison with state-of-the-art works

	Ref. [5]	Ref. [7][a]	Ref. [8][a]	This work[a]
Design method	ASIC	ASIC	ASIP	ASIP
Technology	40 nm	28 nm	28 nm	28 nm
Schedule	Layered	Flooding	Layered	Layered
Parallelism	84 × 84	42 × 672	42 × 336	42 × 672
Frequency [MHz]	850	130	500	400
Iterations	3	3.75	3	3
Throughput [Gbit/s]	5.05	6	5.4	7.07
Core area [mm^2]	0.18	0.63	0.087	0.126
Supply voltage [V]	None	0.7	0.9	0.8
Power [mW]	None	38	57.4	53.6
Energy efficiency [pJ/bit/iteration]	None	1.7	3.5	2.5
Area efficiency [Gbit/s/mm^2]	57.3	9.5	61.7	54.5

[a]Figure of merit measured for coding rate 1/2.

The energy efficiency and area efficiency comparison is further summarised in Fig. 3. Compared with [7], our work shows close energy efficiency while showing a factor of 5.7 gain in terms of area efficiency, taking benefit of the layered schedule. If two cores are instantiated, more aggressive DVFS can be applied for the 6 Gbit/s mode to further improve energy efficiency with certain scarification of area efficiency.

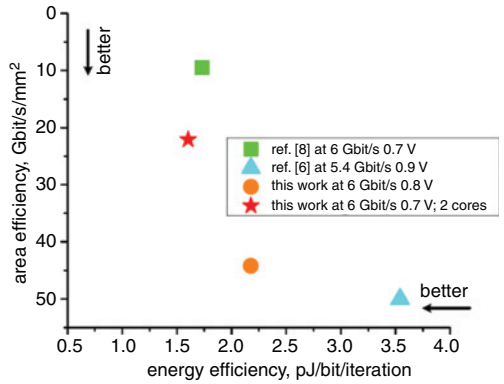

Fig. 3 *Energy and area efficiency comparison with state-of-the-art works for 802.11ad decoder*

Conclusion: A row-based LDPC decoding processor targeting multi-Gbit/s throughput using a layered schedule has been presented. It offers flexibility and helps with the speed up time to market for the high throughput LDPC design. The implementation results of the instantiation for the 802.11ad standard not only show fast decoding speed but also high-area and low-energy efficiency. This Letter also indicates that a multi-core solution or frame pipelined row-based layered schedule will be a good candidate for 10+ Gbit/s LDPC application.

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One or more of the Figures in this Letter are available in colour online.

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