An energy efficient 18Gbps LDPC decoding processor for 802.11ad in 28nm CMOS

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***Abstract*—The design of multi-Gbps LDPC decoder has become a hot topic in recent years as the demand of transformation towards 5G. An energy efficient 18Gbps LDPC decoder based on LDPC ASIP with half layer paralleled architecture is proposed. The feasibility of the design is proven by its demonstrator silicon in 28nm CMOS technology, with a record energy efficiency of 18.4 pJ/decoded bit and area efficiency of 23.8 Gbps/mm^2 for the ½ coding rate working at 18.4Gbps. With frequency, voltage scaling and multi-core management, the decoder supports a wide range of throughput, from 1.8Gbps to 18.4Gbps. The measurement results show the ASIP based design not only provides an energy efficient high speed solution but also be competitive with published ASIC solution at low and medium throughput scenarios.**

Keywords— LDPC; 802.11ad; processor;

I. INTRODUCTION

Low density parity check codes (LDPC) is becoming popular and widely adopted in many new wireless standards because of its high error correction capability and matured solution of implementation. Moving to 5G telecommunication network, multiple standards are trying to push their throughput higher towards multi-Gbps. In the meanwhile, the 60GHz communications with multi-Gbps date rate for local area networks (WLAN) and the wireless personal area networks (WPAN) are almost ready for the market. Even more than 10Gbps data rate communication scenarios are already considered for the next generation of 60GHz communication, such as ultra-short range communication, data center application, video/mass-data distribution and etc. Since the error correction is an essential component in baseband and works at bit rate, the design of high speed, such as 10+Gbps, LDPC decoder has become a hot topic in recent years. However, designing a LDPC decoder with multi-gigabit throughput while maintaining low power consumption and low area which is still suitable for portable device is a big challenge.

In this paper, we proposed an energy efficient high speed LDPC decoder with scalable throughput from 55 Mbps to 18Gbps, which is suitable for all IEEE 802.11ad application scenarios, even for the next generation of 60GHz communication with 10+ Gbps throughput demand. In section II, we first detail a high throughput LDPC decoding processor, using a half layer paralleled architecture to provide better tradeoff between area, power consumption and the throughput. The proposed processor fits different standards and different throughput requirement for each by changing the decoding parallelism. Then a multi-core solution of the proposed processor instantiated for the 802.11ad application is detailed. Multi-core implementation combing with voltage and frequency scaling enable an energy efficient 802.11ad LDPC decoder at low throughput is further proposed. The measurement results are presented in section III. Conclusion is summarized in Section IV.

II. PROPOSED ARCHITECTURE

A. Half-layer paralleled LDPC decoding processor

Message passing is the most popular decoding algorithm for LDPC codes. The message passing has two different forms: flooding [1] and layered [2], based on different scheduling of messages passed between the check nodes and bit nodes. Compared to the flooding decoding, the layered decoding is preferable by the industry due to fast convergence speed and less hardware (HW) cost. The intermediate utilization of the posterior information enables the fast convergence speed. However, this property also posts implementation constraint on layer decoding for high throughput application. Expending processing parallelism is a straightforward way to increase the decoding speed. In a row-based mapping architecture [3], the number of bit node function unit (VFU) is equal to the length of the code word and the number of check node function unit (CFU) is equal to the size of sub-matrix for quasi-cyclic (QC)-LDPC codes. Pipeline is another method to increase decoding speed. However, pipeline between each layer decoding is prohibitive for the row-based mapping architecture due to former explained reason.

In order to achieve high throughput and high utilization of HW, a half layer paralleled architecture [4] is proposed and an application specific instruction-set processor (ASIP) based on this architecture is designed by using Synopsys IP Designer. The high speed LDPC decoding processor can be instantiated for 802.11ad, 802.11ac/802.11n and other standards with QC-LDPC codes. In the rest of this paper, we will focus on the 802.11ad application only.

The LDPC codes of 802.11ad is quasi-cyclic of each Z=42 sub-matrix and it supports four coding rates, i.e. 1/2, 5/8, 3/4 and 13/16, with coding length of 672. The

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architecture of the half layer paralleled LDPC decoder is show in Fig. 1, in which there are 381 VFU and 42 check node function unit (CFU). Only half of the bit nodes are mapped to VFU, which is mapped to 8 slices. Each slice consists of data memories, barrel shifter and arithmetic computation elements, with a parallelism degree of 42. The CFU consists of the min-sum (MS) block and output block, which is shown on the right side in Fig. 1. Each CFU processes maximum 8 a priori information which is sent from the 8 different slices. Since each time, the CFU gets the check node information: minimum and sign, among the bit nodes from half of the code word, two half layer processing is required to get a final minimum and sign information of a certain layer.

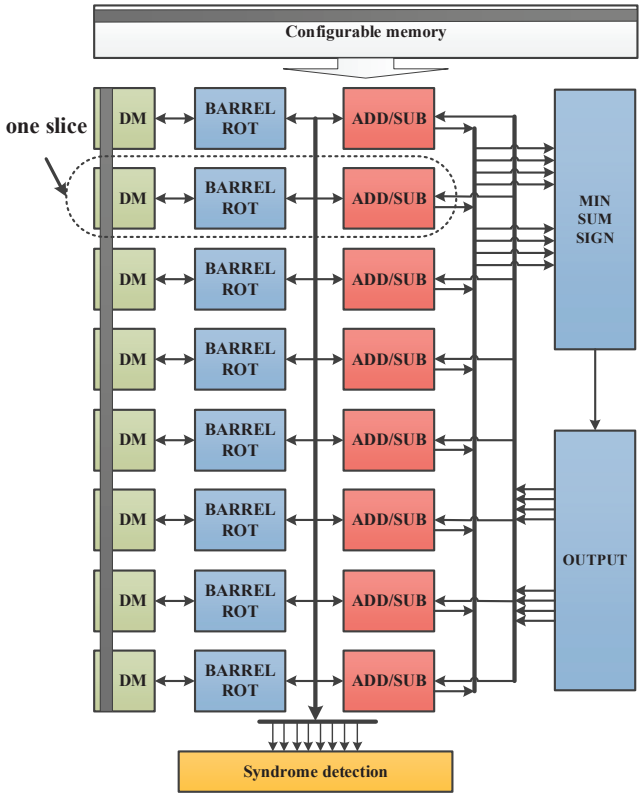

Fig. 1. Architecture of the half layer paralleled LDPC processor

Every layer decoding takes 5 cycles. Since there are no memory access conflict among two different half layers, a half layer level pipeline is applied to increase the HW utilization and thus to increase the throughput. One cycle overlap is allowed between two consecutive layer decoding, which further increases the throughput. The details of timing and firmware mapping is detailed in Fig.2.

The architecture of the VLIW/ SIMD processor are is described in nml file in the IP Designer. There are 4 different instruction slots:

1.) scalar : initialization and control
2.) load-rotate-subtract: load *a posterior* information, rotation, subtraction
3.) min search: minimum search among half layer, overall sign and minimum calculation
4.) output-add-store: updated extrinsic information generation, addition, store the updated posterior information and syndrome calculation

The number of cycles to perform certain iterations can be described as: (4 × Nlayer) × Niter + 1, which leads to a payload throughput of 6.7Gbps with 5 iteration for the coding rate 13/16 of 802.11ad standard, working at 620MHz.

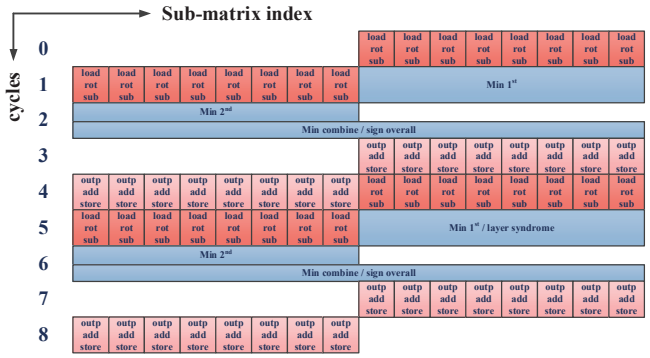

Fig. 2. Firmware and timing of two consecutive layer decoding

Since the decoding latency is in linear with the number of layers to be processed, the throughput decreases significantly at low coding rates. However, the properties of the parity check matrix of low coding rate in the 802.11ad standard enable two different layers decoding to be performed within 5 cycles to increase the throughput. In this case, two layers are combined as one virtual layer. Each layer is processed as half layer decoding of one virtual layer. The parity check matrix of the coding rate ½ with two layers combined, which are marked with similar color, is shown in Fig. 3.

However, to map 8 *a priori* information in each layer or virtual layer to the 8 APP (*posterior information*) memory is not straightforward, especially for the ones which are highlighted in the dotted boxes in Fig. 3.

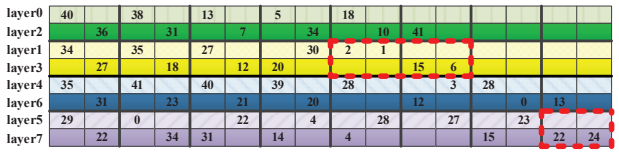

Fig. 3. Party check matrix of the 802.11ad standard of coding rate 1/2

Applying certain column re-ordering when the information of every 8 bit node vectors are mapped to the 8 APP memories makes the routing from APP memory to VFU and the re-routing from CFU to VFU regular as shown in Fig.1.

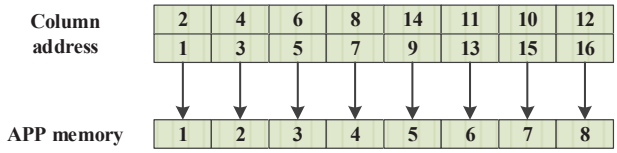

Fig. 4. Column re-order to enable regular connection between VFU and CFU for coding rate 1/2

B. Multi-cores solution

In order to provide high throughput for the 802.11ad standard and potential higher throughput demanding scenario, four processors configured as 802.11ad mode are instantiated as shown in Fig.5. To provide a wide range coverage of decoding throughput, each processor can be switched on and off separately. Moreover, the supply voltage of the main core is also tunable to provide a voltage and frequency scaling feature.

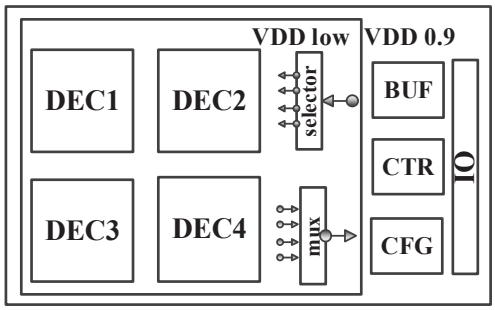

Fig. 5. Multi-cores architecture

III. Measurement Results

To demonstrate the energy efficient high speed LDPC decoder, a demonstrative chip is designed and fabricated in 28nm CMOS process technology. Fig. 6 shows the micrograph of the test chip and its characteristic in area.

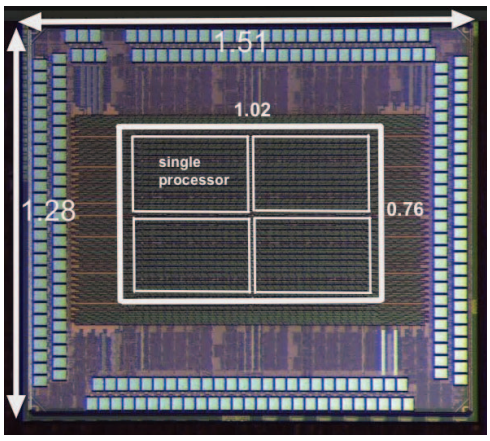

Fig. 6. Chip micrograph (dimension in mm)

The chip is divided into two parts, each operating on different frequency. One is the core which includes four processors working at tunable voltage and frequency and the other one includes the IO storage and control logic, which are working at comparable low I/O frequency and under constant 0.9V supply voltage. The IO storage is necessary to make sure a real time measurement of the core at high speed match the IOs working at low or medium frequency.

A. Implementation results

The core is synthesized at 630 MHz and when it is configured at this working frequency it can reach 18.4Gbps payload throughput for the 1/2 coding rate with maximum 4 iterations. All the four coding rates are supported and the corresponding BER performance under AWGN channel is shown in Fig. 7. By voltage and frequency scaling (VFS) and combined with core selection, the decoder can handle a payload throughput from 1.8 Gbps to 18.4Gbps. The measurement results show that with 4 cores working at low frequency is much more energy efficient then with 1 core working at high frequency. So when the decoder works at medium or low throughput mode, we choose to enable 4 cores working at low frequency.

More detailed measurement results for the 1/2 coding rate working at BER 10^-6 at different throughput scenarios are listed in Table 2 and shown in Fig. 8.

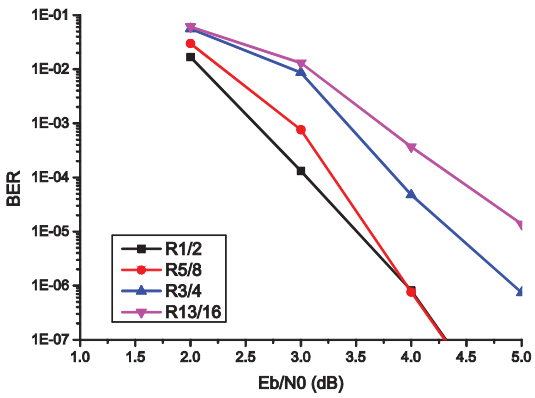

Fig. 7. Measured BER performance under AWGN channel QPSK

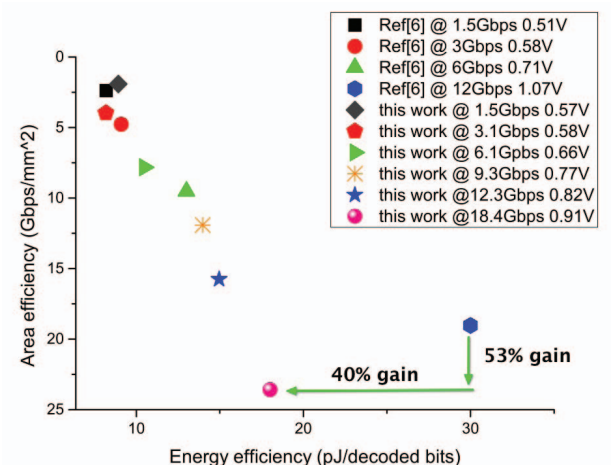

Fig. 8. Energy and area efficiency comparison with the Ref. [6] at different throughput scenarios

B. Comparision with the state of the art

The comparison of the design and implementation results with the state-of-the-art LDPC decoders for the 802.11ad standard is shown in Table 1. In [4], partial paralleled and partial-layer-pipelined architecture is adopted, it increases the throughput by carefully re-ordering the parity check matrix. Ref [5] details the half layer paralleled architecture of the proposed LDPC decoding processor. To the authors' knowledge, Ref. [6] is the only published taped-out design for 802.11ad till now. It uses row-based and frame-pipelined architecture with flooding schedule and offers wide range of throughput by using voltage and frequency scaling (VFS). The decoding speed of the flooding schedule is almost half of the layered schedule. So even though Ref.[6] uses frame level pipeline to compensate the low speed of flooding schedule, the maximum throughput is limited. It can reach 12Gbps but with over boosted supply voltage of 1.07V. The half layer paralleled architecture is area efficient design due to high hardware utilization. So the multi-core of the ASIP processor based on this architecture is a good solution for high throughput application. Compared to Ref. [6], our design can provide higher throughput with better energy efficiency and similar area efficiency. The energy and area efficiency comparison between our work and Ref. [6] at different throughput scenarios are shown in Fig. 8. Our solution is more efficient both in energy and area when compared with Ref. [6] at each's highest throughput mode. The comparison under same throughput mode also shows that our solution has better energy efficiency at high throughput scenarios (above 1.5Gbps) due to more efficient utilization of hardware resource with layer decoding and higher decoding parallelism, however it is slightly worse at low throughput scenarios because of the superior performance property of UTBB FDSOI at low supply voltage which is adopted in Ref. [6] and the voltage of our design and frequency can't be lower.

	Ref.[4]	Ref.[5]	Ref.[6]*	This work*
Design method	ASIC	ASIP	ASIC	ASIP
Technology	40nm	28nm	28nm	28nm
Schedule	layered	layered	flooding	layered
Parallelism	84 x 84	42 x 336	42 x 672	42 x 336
Frequency[MHz]	850	500	130	470
Iterations	3	3	3.75	2 (avg.)
Throughput[Gbps]	5.05	5.4	12	18.4
Core area[mm^2]	0.18	0.087	0.63	0.78
Supply voltage [V]	None	0.9	1.07	0.9
Power[mW]	None	57.4	179.9	166
Energy efficiency [pJ/decoded bit]	None	21.2	29.9	18.00
Area efficiency [Gbps/mm^2]	57.3	61.7	15.38	23.58

Table. 1 The implementation results comparison with the state-of-the-art works (*figure of merits is measured for coding rate ½ @ 12Gbps modes)

	1.8G	3G	6G	9G	12G	18G
No. cores	4	4	4	4	4	4
Voltage[V]	0.57	0.58	0.66	0.77	0.82	0.90
Frequency[Mhz]	100	100	200	300	400	470
Power[mW]	6.7	12.7	32	65	92	170
Energy eff. [pJ/decoded bit]	8.92	8.19	10.49	13.98	14.96	18.4

Table 2. Implementation results of our decoder of ½ coding rate under AWGN high SNR with average iteration of 2

IV. CONCLUSION

This paper presents an energy efficient multi-Gbps LDPC decoder which is based on four ASIP LDPC processors using a half layer paralleled architecture. When this processor is configured for the 802.11ad standard, it can achieve a highest throughput of 18.4Gbps with an energy efficiency of 18 pJ/decoded bit and an area efficiency of 23.58 Gbps/mm^2 for the 1/2 coding rate at 2 iterations under high SNR, which provides 40% energy efficiency gain and 53% area efficiency gain when compared to the state-of-the-art ASIC solution working at 12Gbps. With voltage and frequency scaling, it also can be configured at low and medium throughput modes while maintaining good energy and area efficiency. The measurement results show that the proposed work provides an energy and area efficient LDPC decoder with flexibility in throughput and it would be a good FEC solution for the 60GHz communication.

REFERENCES

[1] R. Gallager, "Low-Density Parity-Check Codes," IRE Tans. Inf. Theory, vol. 7, pp. 21–28, 1962.

[2] D. Hocevar, "A reduced complexity decoder architecture via layered decoding of LDPC codes," in Proc. IEEE Workshop on Signal Process. Syst. (SiPS), Oct. 2004, pp. 107–112.

[3] S. Philipp, W. Christian, W. Norbert, A. Matthias, "Design Space of Flexible Multigigabit LDPC Decoders", Hindawi, VLSI Design, vol. 2012, ID 942893, Feb. 2012.

[4] Balatsoukas-Stimming, A., Preyss, N., Cevrero, A., Burg, A., Roth, C.: 'A parallelized layered QC-LDPC decoder for IEEE 802.11ad', New Circuits and Systems Conference (NEWCAS), June 2013

[5] L. Meng, F. Naessens, L. Min, P. Deback, C. Desset, ect.: "A processor based multi-standard low-power LDPC engine for multi-Gbps wireless communication", Global Conference on Signal and Information Processing (GlobalSIP), 2013 IEEE , pp.1254,1257, Dec. 2013

[6] M. Weiner, M. Blagojevic, S. Skotnikov, A. Burg, P. Flatresse, B. Nikolic, "A scalable 1.5-to-6Gb/s 6.2-to-38.1mW LDPC decoder for 60GHz wireless networks in 28nm UTBB FDSOI", Solid-State Circuits Conference Digest of Technical Papers (ISSCC), pp.464,465, 2014 IEEE International, Feb. 2014