Yanxiang **Huang**

PH.D RESEARCHER OF IMEC & KU LEUVEN

DIGITAL CIRCUITS AND SYSTEMS · COMPUTE ARCHITECT · RESILIENT DIGITAL SIGNAL PROCESSING

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Education

KU Leuven (University of Leuven)

Leuven, Belgium

PH.D IN ELECTRICAL ENGINEERING

Nov. 2013 - Sept. 2017

- Fully sponsored by the imec Ph.D scholarship.
- Performed in the perceptive system group, imec.
- Ph.D dissertation: cross-level optimization of robust and efficient digital circuits and systems (supervised by Prof. Wim Dehaene and Prof. Liesbet Van der Perre).

Eindhoven University of Technology (TU/e)

Eindhoven, Netherlands

M.S. IN ELECTRICAL ENGINEERING

Sept. 2011 - Sept. 2013

- GPA: 8.0/10.0 (top 15%)
- Tuition fee waived and allowance sponsored by the TU/e Amandus H. Lundqvist Scholarship Program (Talent Scholarship Program).
- Focused on embedded system, signal processing, digital IC, and computer architecture.
- Master thesis: High speed and low power DSP implementation using carry-save numbers (supervised by Prof. José Pineda de Gyvez).

Zhejiang University

Hangzhou, China

BACHELOR'S DEGREE IN ENGINEERING WITH A SPECIALTY OF ELECTRONIC AND INFORMATION ENGINEERING

Sept. 2007 - June 2011

- GPA: 3.68/4.0 (top 20%)
- Admitted without entrance exam for outstanding performance in high school physics contest (1st Prize in the Chinese Physics Olympiad, 1%).

Professional Experience

KU Leuven

Gent, Belgium

RESEARCHER

Oct. 2017 - Now

- Research and develop on smart Internet-of-Things (IoT) sensor nodes

Imec

Leuven, Belgium

PH.D RESEARCHER

Nov. 2013 - Sept. 2017

- Research and develop on robust low power digital circuit and system, in IoT computing, digital accelerators, and wireless communication domains.
- Investigated cross-level optimization from system to architecture, and to circuit technology for digital systems.
- In charged of 1 tape-out, and co-designed 2 tape-outs, in 28nm CMOS, including CORDIC digital computing accelerators, 7 Gbps digital front-end , and 30 Gbps LDPC decoder.

Central Research Division, NXP semiconductors

Eindhoven, Netherlands

RESEARCHER (M.S. GRADUATION INTERN)

May 2012 - June 2013

- Researched on high-speed digital circuit for signal processing. (M.S. thesis rated 8.5/10)
- Designed arithmetic units for multi-standard digital radio front-end, and frequency divider.

ACTLab (iCareNet), TU/e *Eindhoven, Netherlands*

Research Assistant (non-paid intern) *Dec. 2011 - May. 2012*

- Designed an algorithm & application (SmartTrainGloves: Monitoring gym training using smart-gloves) to coach Gym exercises by wireless sensors and smart-phones.
- Developed an Android smart-phone application to visualize results in real-time.

Peer Reviewed Publications

Journal Publications

[1] **Y. Huang et al.** Computation-skip Error Mitigation Scheme for Power Supply Voltage Scaling in Recursive Applications. *Journal of Signal Processing Systems (JSPS)*, 84(3):413–424, September 2016. ISSN: 1939-8018. DOI: 10.1007/s11265-015-1096-z.

[2] **Y. Huang et al.** Fine-grained hardware switching scheme for power reduction in multiplication. *Electronics Letters*, 52(16):1374–1375, August 2016. ISSN: 0013-5194. DOI: 10.1049/el.2015.3828.

[3] **Y. Huang (co-author)**. Energy-Efficient Digital Front-End Processor for 60 GHz Polar Transmitter. *Journal of Signal Processing Systems (JSPS)*, 1939(8115):1–13, December 2016. ISSN: 1939-8018. DOI: 10.1007/s11265-016-1213-7.

[4] **Y. Huang (co-author)**. Area and energy efficient 802.11ad LDPC decoding processor. *Electronics Letters*, 51(4):339–341, February 2015. ISSN: 0013-5194. DOI: 10.1049/el.2014.4263.

[5] **Y. Huang et al.** A 13bits 4.096GHz 45nm CMOS digital decimation filter chain with Carry-Save format numbers. *Microprocessors and Microsystems*, 39(8):869–878, November 2015. ISSN: 01419331. DOI: 10.1016/j.micpro.2014.11.003.

Book Chapters

[6] **Y. Huang et al.** Implementation Studies of Multi-rate Systems. In *Advances in Multirate Systems*, pages 1–33. Springer, 2018. ISBN: 978-3-319-59273-2.

Conferences and Workshop Inproceedings

[7] **Y. Huang et al.** Massive MIMO processing at the semiconductor edge: Exploiting the system and circuit margins for power savings. In *2017 IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP)*, pages 3474–3478, New Orleans, U.S. IEEE, March 2017. ISBN: 978-1-5090-4117-6. DOI: 10.1109/ICASSP.2017.7952802.

[8] **Y. Huang (co-author)**. Lousy processing increases energy efficiency in massive MIMO systems. In pages 1–5, Oulu, Finland, June 2017. DOI: 10.1109/EuCNC.2017.7980739.

[9] **Y. Huang et al.** A 28 nm CMOS 7.04 Gsps polar digital front-end processor for 60 GHz transmitter. In *2016 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, pages 333–336, Toyama, Japan. IEEE, November 2016. ISBN: 978-1-5090-3699-8. DOI: 10.1109/ASSCC.2016.7844203.

[10] **Y. Huang et al.** Partial Computation-skip Scheme for Power Supply Voltage Scaling. In *1st Workshop On Approximate Computing, HiPEAC (WAPCO)*, Amsterdam, Netherlands, 2015.

[11] **Y. Huang (co-author)**. < 30 mW rectangular-to-polar conversion processor in 802.11 ad polar transmitter. In *2015 IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP)*, pages 1022–1026, South Brisbane, Australia. IEEE, April 2015. ISBN: 978-1-4673-6997-8. DOI: 10.1109/ICASSP.2015.7178124.

[12] **Y. Huang (co-author)**. An energy efficient 18Gbps LDPC decoding processor for 802.11ad in 28nm CMOS. In *2015 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, pages 1–5, Xiamen, China. IEEE, November 2015. ISBN: 978-1-4673-7191-9. DOI: 10.1109/ASSCC.2015.7387473.

[13] **Y. Huang et al.** Computation-skip error resilient scheme for recursive CORDIC. In *2014 IEEE Workshop on Signal Processing Systems (SiPS)*, pages 1–6, Belfast, Northern Ireland. IEEE, October 2014. ISBN: 978-1-4799-6588-5. DOI: 10.1109/SiPS.2014.6986061.

[14] **Y. Huang (co-author)**. Gbps Throughput Architecture for Turbo Decoder. In *Information Theory in the Benelux and The 4th Joint WIC/IEEE Symposium on Information Theory and Signal Processing in the Benelux*, page 178, Eindhoven, Netherlands, 2014.

[15] **Y. Huang et al.** A 13 bits 4.096 GHz 45 nm CMOS digital decimation filter chain using Carry-Save format numbers. In *31th Norchip Conference*, pages 1–4, Vilnius, Lithuania. IEEE, November 2013. ISBN: 978-1-4799-1647-4. DOI: 10.1109/NORCHIP.2013.6702042.

Poster presentations

[16] **Y. Huang et al.** An algorithm to identify cornerstones of digital circuits. In *ACM/IEEE Design Automation Conference (DAC), Work-In-Progress*, Austin, U.S., 2016.

Thesis publications

[17] **Y. Huang**. *Cross-Layer Optimization for Power-Efficient and Robust Digital Circuits and Systems*. PhD thesis, KU Leuven, 2017, pages 1–190.

[18] **Y. Huang**. *Carry-Save Arithmetic for High-Performance DSP*. Master of Science Thesis, Eindhoven University of Technology, 2013, pages 1–12.

Patents

- **Y. Huang (co-author)**, "Digital Frontend System for a Radio Transmitter and a Method Thereof", imec, KU Leuven R&D, 2016, **US Grant** No. 09825654. **EU** Publication No. EP 3232629 A1.
- **Y. Huang et al**, "Error Resilient Digital Signal Processing Device", imec, KU Leuven R&D, 2015. **US** Publication No. 20160110492 A1. **EU** Publication No. EP 3012975 A1.

Professional Activities

Committees

2017 **TPC member,** 13th Conference on PhD Research in Microelectronics and Electronics (PRIME 2017)

2017 **TPC member,** The Second International Conference on Advances in Signal, Image and Video Processing (SIGNAL 2017)

Reviewers

2016-17 **IEEE Transactions on Circuits and Systems-1: Regular Papers (TCAS-I),** 11 reviews

2014-17 **IEEE Transactions on Circuits and Systems-1: Express Papers (TCAS-II),** 7 reviews

2017 **IEEE Transactions on Wireless Communication (TWC),** 1 reviews

2016 **Spinger Journal of Signal Processing Systems (JSPS),** 2 reviews

2017 **IEEE International Conference on Communications (ICC),** 5 reviews

2016 **IEEE International Workshop on Signal Processing Systems (SiPS),** 4 reviews

2017 **13th Conference on PhD Research in Microelectronics and Electronics (PRIME 2017),** 4 reviews

2017 **2nd International Conference on Advances in Signal, Image and Video Processing (Signal),** 1 reviews

2017 **2nd International Conference on Advances in Signal, Image and Video Processing (Signal),** 1 reviews

2017 **20th International Symposium on Wireless Personal Multimedia Communications,** 2 reviews

Teaching Activities

Thesis co-guidance

2016	**M.S. thesis Habib Khalid,** Signal processing for machine learning	*imec, Belgium*
2016	**M.S. thesis Micaela Bortas & Sara Gunnarsson,** Massive MIMO	*KU Leuven, Belgium*
2015	**M.S. thesis Zhijie Xu,** high-speed DSP	*imec, Belgium*
2014	**M.S. thesis Yuzhu Gai,** mm-wave car radar FPGA prototype	*imec, Belgium*
2014	**M.S. thesis Antonio Callejón,** high-speed Turbo error correction code decoder	*imec, Belgium*

Course teaching assistant

2015,6	**Project & development embedded systems and multimedia (H09M0A),** Guided DSP lab sessions to implement and optimize RSA (en)decryption and audio (en)decoding	*KU Leuven, Belgium*
2014,6	**Advanced platform architectures and mapping methods for embedded applications (H05B9B),** Helped to preapare and conduct exercise sessions	*KU Leuven, Belgium*

Projects

Imec

Leuven, Belgium

Digital signal processing for machine learning — *Nov. 2016 - Sept. 2017*

- Supervised master thesis on accelerating hand-gesture recognition process captured by mm-wave radar, for learning on Nvidia GPU TX1 SoC, and for interference on Xilinx Znyq 7000 FPGA.
- Utilized PCA algorithm for baseline, and applied DNN with LSTM (using Caffe in Python and C++ and CUDA); Currently performing fixed-point refinement for power saving.

Imec

Leuven, Belgium

Finding corner-stones in digital circuits — *Sept. 2015 - Dec. 2016*

- Proposed a novel algorithm to automatically pick out critical components in digital circuits.
- Modeled all flip-flops' contribution to circuit output. Iterative graph traversal to solve the large sparse linear equations model.
- Verified the efficiency and effectiveness of the algorithm (using Python, Verilog parser, and json) for larger benchmark circuits (FFT, LDPC, ISCAS'89, ITC'99).

Imec

Leuven, Belgium

DFE for 60GHz polar transmitter — *Mar. 2015 - July 2016*

- Designed the world's first Digital Front-End (DFE) for wide-bandwidth 60GHz polar transmitter (running at 3.52 GHz).
- Processed in 28nm. Tested the DFE with FPGA, for QAM-16 communication.

Imec

Leuven, Belgium

Low-power execution unit for processors — *Jan. 2015 - June 2015*

- Proposed a novel & universal fine-grained hardware switch scheme, to reduce power for multiplier unit, in general purpose processor, which exploits reduced world-length opportunities.
- Benchmarked on industrial standard tasks (communication, matrix operations, recognition), with mork1x OpenRisc micro-processor simulator (in C++ and Verilog). Demonstrated 11% power saving for typical Cormark applications.

Imec

Leuven, Belgium

LDPC decoder — *Mar. 2014 - May 2017*

- Designed high-throughput (up to 30 Gbps) LDPC decoders for IEEE 802.11ad standard.
- Contributed in the 28nm tape-out of a world-class-performance ASIP 802.11ad LDPC decoder. Tested the performance and variability for communication with FPGA.
- Proposed a novel kernel algorithm (approximation min-sum), which reduces kernel area by 20%. Verified the proposed algorithm in i) Matlab, ii) bit-accurate C++ model, iii) Verilog gate-level simulation.
- Designed & implemented a new ASIC LDPC decoder (until P&R), which improves throughput/area by 4.5 times, and energy/bit by 2 times (by data-flow memory optimization, frame-level pipelining, coarse- & fine-grained clock-gating).

Imec *Leuven, Belgium*

Error resilient DSP *Nov. 2013 - Jan. 2016*

- Proposed a scheme to reduce power for DSP by voltage scaling, and mitigate errors introduced by CMOS variability.
- Built timing-error detection and correction cells in RTL level. Verified the scheme by library characterization and physical simulation.
- Processed & verified in 28nm CMOS CORDIC accelerator.

NXP semiconductors *Eindhoven, Netherlands*

High-speed data-path in DSP *May 2012 - June 2013*

- Investigated micro-architecture solutions for high-speed signal processing in RTL level.
- Designed arithmetic units (adders, adders tree, multiplier-accumulators), that outperforms State-of-the-Art EDA tools. Optimized delay-area-power trade-offs in ASIC for different industrial DSP blocks, e.g. multi-standard digital radio front-end, and frequency divider (using RC, DC, Encounter, and Primetime). Developed automation tools to generate VHDL from Matlab.

ACTLab, TU/e *Eindhoven, Netherlands*

Smart train gloves *Dec. 2011 - May 2012*

- Developed an algorithm & application to capture and assist gym exercises, using wireless sensors and smart-phones.
- Captured 3-D acceleration data from sensors SoC. Acquired exercise data via ANT wireless communication.
- Analyzed data and trained model on PC (Matlab). Developed Android smart-phone applications (java and html), to count reps and detect incorrect gestures in real-time.

Skills

Programming Matlab, C/C++, Python, VHDL/verilog, Java, Bash/Tcl/Pearl, CUDA, SystemC, Assembly

OS Windows, Unix, OSX, openRISC

Miscellaneous FPGA, DSP, MCU, iOS & Android dev.

Interests

Professional algorithm implementation, digital hardware, low-power IC, high-performance DSP, computer arch.

Leisure FPGA/DSP programming, machine learning implementation, smart-phone app develop